Exhibit C

SEARCHER: JAMES W. MOFFITT

SEARCH REQUEST NO. SA8-99-0443

SEARCH REPORT FOR: RANDALL J. BLUESTONE

I B M C O N F I D E N T I A L

What Feature(s) Were Searched For?

A process for predicting single reference residency in a LRU cache and using that information to model the utility of keeping prefetched data for I/O streams which are expected to benefit from cache prestaging.

Field of Search:

MANUAL		DATABASES				
Cl/Sub(s)	Cl/Sub(s)	U.S.	Foreign	IBM	Literature	Other
711/133		X WEST	X WPAT	X TDBS	INSPEC	
711/136		LEXIS	X JAPIO	IBMB	COMPENDEX	
711/137		CLAIMS		X DOSS		
712/237		USP				
		QPAT				

☒ **Summary of Search Strategies Attached**

RELATED ART				BACKGROUND ART			
Ref.	Patent No.	Date	Cl/Sub	Ref.	Patent No.	Date	Cl/Sub
A.	US 5706467	1-06-98	711/136	K.			
B.	US 5701426	12-23-97	711/136	L.			
C.	US 5537568	7-16-96	711/136	M.			
D.	US 5452440	9-19-95	711/133	N.			
E.	US 4980823	12-25-90	711/136	O.			
F.	US 4509119	4-02-85	711/136	P.			
G.				Q.			
H.				R.			
I.				S.			
J.				T.			

Ref.	Non-Patent Literature	Ref.	Non-Patent Literature
aa.	Research Disclosure (RD) 297096 dated	ae.	
	1-10-89; 1 page RD 297096		
ab.	CMG '87 Proceedings, pages 9-15 by	af.	
	by McNutt and Murray		
ac.	Proceedings of CMG '91, pages 203-211	ag.	
	by McNutt		
ad.	CMG Transactions-Winter 1993, Pages 13-21 by McNutt	ah.	
	CMG = Computer Measurement Group		

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IBM CONFIDENTIAL

How Does Each Of The Related Art References Correspond To The Search Feature? (Claims - If Validity/Clearance)

Ref. A discloses a shared memory system which uses a "least recently used" cache and detects the occurrence of a sequential access for prefetching data.

Ref. B discloses a method of detecting a cache miss and predicting a succeeding cache miss which is forced to a "least recently used" status.

Ref. C discloses the use of a LRU cache with sequential accessing and prefetching.

Ref. D discloses producing an exact analytical model which can be used to calculate the cache hit rate for combinations of various data sets, given a specific size of an LRU stack.

Ref. E discloses sequential prefetching of cache lines using a prediction scheme using an LRU cache.

Ref. F discloses the use of a normal LRU buffer chain and a sequential LRU buffer chain for sequential and random processes.

Ref. aa discloses a LRU cache for prefetching predictable memory accesses and pre-staging the sequential next line upon a miss.

Refs. ab,ac,and ad (abstracts only) are cited in col. 4 of Ref. D above and refer to "single reference residency time".

What Feature(s) Does the Background Art Provide?

Which Feature(s) Were Not Found?

The search fail to find any references that mixes sequential prefetches and random access data in a preexisting LRU cache. ?

Other Comments

Examiner G. Gossage was consulted for Classes 711 and 712.

Full copies of Ref. aa,ab, and ac were not available. If needed they can be ordered thru the WAIPL office in Arlington VA.

Signature James W Moffett

Date Returned to WAIPL 2-7-00

*** *** DOCUMENT NO. AAA87A003649 *** ***
TITLE A Multiple Workload Approach to Cache Planning. July 1987.
ORDER 87A 03649
LOCATION GPD- Santa Teresa
AUTHOR McNutt, B. Murray, J. W.
REPORT TR-03.305
ABSTRACT 22p. Cached controllers can provide a powerful and cost-effective tool for speeding up the I/O activity at an installation. This is true even if the cache is simply installed and turned on. Provided that a large enough amount of cache memory is provided, no particular planning is required to obtain good results.

Long-term planning can, however, enhance the cost-effectiveness of cache and can simplify the cost-justification process. The purpose of this paper is to introduce a set of techniques which may be helpful in choosing a strategy for the use of cache which best meets the needs of a given installation, if a large number of possible options is being considered. This is done by breaking down the data to be cached into workload-related volume groups, or pools. For example, an installation might be considering the purchase of either one, two, or three cached controllers, which would be used to cache some subset of the key system data, the TSO user data, and three data bases of various types. For each cache, a choice among several memory sizes must also be made. An approach to this problem is introduced in which the locality of reference is estimated separately for each individual pool which may share the use of a cached controller. Requirements for cache memory are also estimated for each pool. The proposed approach then allows these estimates to be applied to shared caches containing any combination of the original pools. This procedure makes possible the efficient examination of a large number of potential cached configurations.

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10/3,IC,BA/2
DIALOG(R)File 351:DERWENT WPI

007809919
WPI Acc No: 89-075031/198910
XRPX Acc No: N89-057082
Memory *cache* for *prefetching* in multi-processor computing system - services predictable memory accesses, uses replacement policy, e.g. FIFO, and has line staging dependent on partic implementations
Patent Assignee: ANONYMOUS (ANON)
Number of Countries: 001 Number of Patents: 001
Patent Family:

Patent No	Kind	Date	Applicat No	Kind	Date	Main IPC	Week
RD 297096	A	19890110					198910 B

Priority Applications (No Type Date): RD 88297096 A 19881220
Language, Pages: RD 297096 (1)

Abstract (Basic): RD 297096 A

Although each processor in a multiple processor system may have its own *cache*, another *cach*is provided at the memory level, designated pre-stage *cache*. The pre-stage *cache* has its own directory, is structured as set-associative and uses a replacement policy, such as *least* *recently* *used* or first in-first out. Upon a *cache* miss, for example, on line L from a processor, another line L' is staged to the pre-stage *cache* if a subsequent *cache* miss to L' is anticipated via some mechanism. Memory access that hits to the pre-stage *cache* will be fetched from there. Line staging to the pre-stage *cache* depends on the particular implementations, e.g. pre-stage the *sequential* next line upon a miss unless other information is available to save the pre-staging.

As variations, the pre-stage *cache* can be read-only used for fetch misses, be provided for each system module, or have a granularity different from line sizes of other *caches*. Pre-staging of data into a pre-stage *cache* may be pre-emptied by more urgent fetching and the pre-stage *cache* mechanism can apply to other *cache* levels.

ADVANTAGE - Very short access time
International Patent Class (Additional): G06F-000/01

DIALOG(R)File 8:Ei Compendex(R)

03685145 E.I. No: EIP93050800293
Title: Simple statistical model of cache reference locality, and its application to cache planning, measurement and control
Author: McNutt, Bruce
Corporate Source: Int Business Machines Corp, San Jose, CA, USA
Source: CMG Transactions n 79 Winter 1993. p 13-22
Publication Year: 1993
CODEN: CMTREK
Language: English
Document Type: JA; (Journal Article) Treatment: A; (Applications); T; (Theoretical)
Journal Announcement: 9310W2
Abstract: The causes of data reuse in storage control cache are often hierarchical. For example, reuse may be caused by repeated requests in the same subroutine; by different routines called to process the same transaction; or by multiple transactions needed to carry out some overall task at the user level. This paper develops a model of cache locality based on the assumption of hierarchical behavior. The model applies the concept of statistical self-similarity, which arises often in the study of fractals, to infer a very simple method of approximating cache miss ratios. The model's approximations are checked empirically against a large number of I/O traces and are shown to be highly serviceable. The model is then applied to the problems of cache miss ratio projection, trace-based measurement of cache miss ratios, and allocation and dynamic management of cache resources. (Author abstract) 9 Refs.

AAA91A005812 DOCUMENT= 2 OF 2 PAGE = 1 OF 2
TITLE A Simple Statistical Model of Cache Reference Locality and its Application to Cache Planning, Measurement and Control. September 1991.
ORDER 91A 05812
LOCATION GPD- Santa Teresa
AUTHOR McNutt, B.
REPORT TR-03.411
ABSTRACT 11p. The causes of data reuse in storage control cache are often hierarchical. For example, reuse may be caused by repeated requests in the same subroutine; by different routines called to process the same transaction; or by multiple transactions needed to carry out some overall task at the user level. This paper develops a model of cache locality based on the assumption of hierarchical behavior. The model applies the concept of statistical self similarity, which arises often in the study of fractals, to infer a very simple method of approximating cache miss ratios. The model's approximations are checked empirically against a large number of I/O traces and are shown to be highly serviceable. The model is then applied to the problems of cache miss ratio projection, trace-based measurement of cache miss ratios, and allocation and dynamic management of cache resources.

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